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001/017

## FACSIMILE COVER SHEET

**TO: Examiner N. Drew Richards, Art Unit 2815**

Company: Assistant Commissioner for Patents  
Fax No.: 703/872-9318

**FROM: Julie G. Cope, Reg. No. 48,624/amm**

Date: November 12, 2002

Pages: 17

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Our Docket No.: MIO 0037 VA

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*Patents, Trademarks and Related Matters*  
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Remarks:

**U.S. Patent Application Serial No. 09/605,293**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicant : David L. Chapek  
Serial No. : 09/605,293  
Filed : June 28, 2000  
Title : SEMICONDUCTOR DEVICES INCLUDING A LAYER OF  
POLYCRYSTALLINE SILICON HAVING A SMOOTH  
MORPHOLOGY  
Docket : MIO 0037 VA  
Art Unit : 2815

Assistant Commissioner for Patents  
Washington, DC 20231

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Sir:

AMENDMENT

This paper is being filed in response to the Office Action mailed on September 11, 2002. Reconsideration is respectfully requested in light of the amendments and remarks below.

**CLEAN VERSION OF THE AMENDMENTS**

(A version of these amendments with markings to show the changes is attached to this paper as a separate appendix.)

At page 11, lines 9-18, the paragraph should read:

A method for making the field effect transistor 50 is shown in Figs. 2A-2C. As an initial step, the layer 72 of the field oxide 74 is formed on the substrate 52 by means of a conventional local oxidation of silicon (LOCOS) process. Next, a gate oxide 54 is formed in substrate 52. The surface of the substrate 52 is then conditioned or pretreated so that the subsequently formed layer 64 of polycrystalline silicon 66 has a smooth morphology. The surface of the substrate 52 is pretreated by implanting hydrogen ions into the surface of the substrate 52 through plasma source ion implantation by the method described above. Fig. 2A shows a layer 64 of polysilicon 66 having been formed on the surface of the substrate 52. The layer 64 of polysilicon 66 covers the gate oxide 54.